What is claimed is:

1. A wiring structure of a semiconductor device comprising,

a first insulating film having plural grooves,

plural wiring films formed such that the films are protruded above tops of the first insulating film among the grooves,

plural barrier films formed on bottoms of the wiring films and up to a higher position than the tops on sides of the wiring films,

first cap films comprising metal films formed on tops of the wiring films, and

a second cap film formed on at least respective sides of the first cap films and the barrier films.

2. The wiring structure of the semiconductor device according to claim 1 wherein the first cap films are formed by electroless plating.

3. The wiring structure of the semiconductor device according to claim 2 wherein the first cap films are metal films containing Co or Ni as a main component.

4. The wiring structure of the semiconductor device according to claim 3 wherein the wiring films are metal films of Cu or metal films containing Cu as a main component.

5. The wiring structure of the semiconductor device according to claim 1 wherein the second cap film is formed on

an entire surface extending from tops of the first cap films to the tops of the first insulating film.

6. The wiring structure of the semiconductor device according to claim 5 wherein the second cap film is an insulating film of Si_xN_y, $Si_xO_yN_z$, or Si_xC_y, or an insulating film containing Si_xC_y as the main component.

7. The wiring structure of the semiconductor device according to claim 1 wherein the second cap film is formed separately for each of the grooves.

8. The wiring structure of the semiconductor device according to claim 7 wherein the second cap film is formed only on respective sides of the first cap films and the barrier films.

9. The wiring structure of the semiconductor device according to claim 8 wherein the second cap film is an insulating film of Si_xN_y, $Si_xO_yN_z$, or Si_xC_y, or an insulating film containing Si_xC_y as the main component.

10. The wiring structure of the semiconductor device according to claim 8 wherein the second cap film is a metal film comprising Ta_xN_y, Ta, or $Ta_xSi_yN_z$.

11. The wiring structure of the semiconductor device according to claim 8 wherein the second cap film is a metal film comprising Ti_xN_y or $Ti_xSi_yN_z$.

12. The wiring structure of the semiconductor device according to claim 8 wherein the second cap film is a metal film comprising W_xN_y or $W_xSi_yN_z$.

13. The wiring structure of the semiconductor device according to claim 1 wherein the barrier films are metal films comprising Ta_xN_y, Ta, or $Ta_xSi_yN_z$.

14. The wiring structure of the semiconductor device according to claim 1 wherein the barrier films are metal films comprising Ti_xN_y or $Ti_xSi_yN_z$.

15. The wiring structure of the semiconductor device according to claim 1 wherein the barrier films are metal films comprising W_xN_y or $W_xSi_yN_z$.

16. The wiring structure of the semiconductor device according to claim 1 wherein the wiring films are concaved with respect to the barrier films.

17. A production method of a wiring structure of a semiconductor device comprising,

forming plural grooves on a first insulating film,

forming a barrier film on the first insulating film,

forming a wiring film on the barrier film in the grooves,

removing the wiring film and the barrier film such that the first insulating film among the grooves is exposed,

forming a first cap film comprising a metal film on the wiring film,

reducing thickness of the first insulating film, thereby protruding the wiring film and the barrier film above a top of the first insulating film, and

forming a second cap film on an entire surface.

18. The production method of the wiring structure of the semiconductor device according to claim 17 wherein the first cap film is formed by electroless plating.

19. The production method of the wiring structure of the semiconductor device according to claim 18 wherein the first cap film is a metal film containing Co or Ni as a main component.

20. The production method of the wiring structure of the semiconductor device according to claim 19 wherein the wiring film is a metal film of Cu or a metal film containing Cu as the main component.

21. The production method of the wiring structure of the semiconductor device according to claim 17 further comprising separating the second cap film for each of the grooves by performing an etching back process to the second cap film.

22. The production method of the wiring structure of the semiconductor device according to claim 21 wherein the second cap film is left only on respective sides of the first cap film and the barrier film.

23. The production method of the wiring structure of the semiconductor device according to claim 22 wherein the second cap film is an insulating film of Si_xN_y, $Si_xO_yN_z$, or Si_xC_y, or an insulating film containing Si_xC_y as the main component.

24. The production method of the wiring structure of the semiconductor device according to claim 22 wherein the second cap film is a metal film comprising Ta_xN_y, Ta, or $Ta_xSi_yN_z$.

25. The production method of the wiring structure of the semiconductor device according to claim 22 wherein the second cap film is a metal film comprising Ti_xN_y or $Ti_xSi_yN_z$.

26. The production method of the wiring structure of the semiconductor device according to claim 22 wherein the second cap film is a metal film comprising W_xN_y or $W_xSi_yN_z$.

27. The production method of the wiring structure of the semiconductor device according to claim 17 wherein the removing the wiring film and the barrier film comprising,

polishing the wiring film using the barrier film as the stopper, and

polishing the wiring film and the barrier film using the first insulating film as a stopper.

28. The production method of the wiring structure of the semiconductor device according to claim 27 wherein the polishing is performed such that a top of the wiring film is concaved with respect to a top of the barrier film in the step for polishing the wiring film and the barrier film.

29. The production method of the wiring structure of the semiconductor device according to claim 27 wherein the barrier film is a metal film comprising Ta_xN_y, Ta, or $Ta_xSi_yN_z$.

30. The production method of the wiring structure of the semiconductor device according to claim 27 wherein the barrier film is a metal film comprising Ti_xN_y or $Ti_xSi_yN_z$.

31. The production method of the wiring structure of the

semiconductor device according to claim 27 wherein the barrier film is a metal film comprising W_xN_y or $W_xSi_yN_z$.